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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR            | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|---------------------------------|---------------------|------------------|
| 09/972,576      | 10/05/2001  | Petrus Hubertus Cornelis Magnee | NL 000549           | 4658             |

7590 11/20/2002

Corporate Patent Counsel  
U.S. Philips Corporation  
580 White Plains Road  
Tarrytown, NY 10591

EXAMINER

IM, JUNGHWA M

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2811

DATE MAILED: 11/20/2002

8

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/972,576

Applicant(s)

MAGNEE ET AL.

Examiner

Junghwa M. Im

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) 6-8 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election of claims 1-5 in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 6-8 are cancelled.

### ***Drawings***

The drawings are objected to. Correction of 26<sup>a</sup> in Figures 3i, and 3m should be 26a.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application.

The objection to the drawings will not be held in abeyance.

### ***Specification***

The disclosure is objected to because of the following informalities.

The specification should include the subheadings with the corresponding sections in order. (See form paragraph 6.01 in MPEP Section 608.01(a) ).

Appropriate correction is required.

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Zambrano (U.S. Pat. No. 5,300,451).

Regarding claim 1, Zambrano shows in Fig. 1, a semiconductor arrangement comprising;  
a substrate having a substrate layer N (second layer from the bottom) with an upper surface and a lower surface, the substrate layer being a first conductivity N;

a first buried layer N<sup>+</sup> (left side portion of the bottom layer N<sup>+</sup>) in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer, and a second buried layer N<sup>+</sup> (right side portion of the bottom layer N<sup>+</sup>) in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer;

a first diffusion region (region designated with P<sup>+</sup> and B) in said first portion of said substrate layer, being of a second conductivity type P<sup>+</sup> opposed to said first conductivity type N<sup>+</sup> and having a first distance I to said first buried layer for defining a first breakdown voltage between said first diffusion region and first buried layer;

a second diffusion region (region surrounded by P1 and P2) in said second portion of said substrate layer, being of a second conductivity type P<sup>+</sup> and having a second distance D to said second buried layer for defining a second breakdown voltage between said second diffusion

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region and second buried layer;

said first distance I being larger than said second distance D such that said first breakdown voltage is larger than said second breakdown voltage (col.3, lines 10-25).

Regarding claim 2, Zambrano shows in Fig. 1, the first diffusion region is a base B of a bipolar transistor and the first buried layer is a collector C of said bipolar transistor.

Regarding claim 3, Zambrano shows in Fig. 1, the second diffusion region is an anode of protection diode and the second buried layer is a cathode of the protection diode (col.3, lines 2-25).

Also see Fig. 2 for the circuit equivalent of Fig. 1.

Regarding claim 4, Zambrano shows in Fig. 1, the first buried layer is connected to said second buried layer, and the first and second buried layers are manufactured in the same step.

Regarding claim 5, Zambrano shows in Fig. 21, the semiconductor arrangement further comprising

a channel stopper region 22 in said second portion of said substrate layer;

the channel stopper region being of said first conductivity type N<sup>-</sup>, for electrically isolating said second portion of said substrate layer within the substrate, wherein said channel stopper regions in between said second diffusion layer 21 and said second buried layer 24 for reducing said second breakdown voltage.

Also, regarding the correlation between a breakdown voltage and a distance defined by a diffused region and a buried layer, see the respective portions of Zambrano's specification such as col. 3, lines 10-35.

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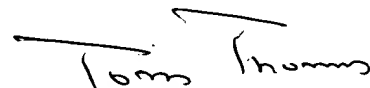
*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMI  
November 12, 2002



TOM THOMAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800